Amendments to the Claims:

The following listing of claims will replace all prior versions and/or listings of claims in the application.

Listing of Claims:

1. (Currently amended) In an isochronous electronic device including at least one processor and a plurality of chips, each said chip associated with a local time counter of a plurality of local time counters, a method for determining a global ordering of events, said method comprising ~~the steps of~~:

detecting an event associated with one of said plurality of chips;

generating a timestamp with said local time counter at the time of the occurrence of said detected event, said timestamp being associated with said event; and

comparing said event and a normalized form of said timestamp with other events and associated normalized timestamps to determine an order of occurrence.

2. (Currently amended) The method of claim 1, further comprising ~~the further steps of~~:

providing a Time Base selected by said processor, said Time Base being a baseline time value; and

transmitting a reset instruction from said processor to said plurality of local time counters associated with said plurality of chips, said plurality of local time counters resetting to a designated time so as to be synchronized with respect to each other.

3. (Currently amended) The method of claim 2 where said processor maintains a record of ~~the~~ an offset between the reset local time counter time and the Time Base.

4. (Original) The method of claim 2 wherein said designated time is the Time Base and said plurality of local time counters are reset so as to indicate the same time as said Time Base.

5. (Original) The method of claim 2 wherein said transmitting of said reset instruction is performed using a simultaneous multicast write operation performed by said processor.

6. (Currently amended) The method of claim 2 wherein the transmitting of the reset instruction is staggered so as to ensure that said resetting occurs simultaneously, said transmitting taking into account ~~any~~ delays caused by network topology.

7. (Currently amended) The method of claim 2, further comprising ~~the further steps of~~:

resetting all of said plurality of chips and an additional chip, said resetting being performed to add the ~~an~~ additional chip that is synchronized with said plurality of chips.

8. (Currently amended) The method of claim 1, further comprising ~~the further steps of~~:

providing a Time Base selected by said processor, said Time Base being a baseline time value;

determining an offset between the time indicated by said Time Base and the time indicated by each of said local time counters associated with said plurality of chips;

recording each offset associated with each said local time counter at a location accessible to said processor; and

normalizing the timestamps associated with said detected events using offsets associated with the local time counter generating the timestamps prior to determining said order of occurrence.

9. (Currently amended) The method of claim 8, further comprising ~~the further steps of~~:

determining an offset for an additional time counter associated with an additional chip in said electronic device following the initial determination and recording of said offsets for said plurality of local time counters associated with said plurality of chips; and

recording said offset at said location accessible to said processor.

10. (Currently amended) The method of claim 1, further comprising ~~the further steps of~~:

providing a Time Base selected by said processor, said Time Base being a baseline time value;

determining an offset between the time indicated by said Time Base and the time indicated by each of said local time counters associated with said plurality of chips;

transmitting each said offset for a local time counter to the chip with which the local time counter is associated;

recording each offset associated with each said local time counter at a location accessible to the chip associated with the local time counter; and

normalizing said timestamp using said offset associated with the local time counter prior to reporting said timestamp and said event to said processor.

11. (Currently amended) The method of claim [[1]] 10 wherein a software timestamp received from ~~the~~ an operating system is associated with said reported event and timestamp.

12. (Original) The method of claim 11 wherein said software timestamp is used in determining said order of occurrence of events.

13. (Original) The method of claim 1 wherein each said chip is associated with a local error register, said local error register recording the occurrence of a hardware error associated with said chip.

14. (Currently amended) The method of claim_1 wherein more than one of said plurality of chips is associated with the same local time counter.

15. (Currently amended) In an electronic device including at least one processor and a plurality of chips, each said chip associated with a local time counter of a plurality of local time counters, said electronic device including a Time Base selected by said processor, said Time Base being a baseline time value, a method for determining a global ordering of events, said method comprising ~~the steps of~~:

determining an offset between the time indicated by said Time Base and the time indicated by each of said local time counters associated with said plurality of chips;

recording each offset associated with each said local time counter at a location accessible to said processor;

receiving notice at said processor of an event detected with one of said plurality of chips, said notice accompanied by a timestamp generated by said local time counter at the time of the occurrence of said detected event; and

normalizing said timestamp using said offset, said normalized timestamp being compared with other reported events and associated normalized timestamps to determine an order of occurrence of said events.

16. (Original) The method of claim 15 wherein more than one reported timestamp is normalized using said offsets prior to determining said order of occurrence.

17. (Currently amended) The method of claim 15, further comprising ~~the further steps of~~:

determining an offset for an additional time counter associated with an additional chip in said electronic device following the initial determination and recording of said offsets for said plurality of local time counters associated with said plurality of chips; and

recording said offset at said location accessible to said processor.

18. (Original) The method of claim 16 wherein a software timestamp received from the operating system is associated with said reported event and timestamp and used in determining said order of occurrence of events.

19. (Original) The method of claim 16 wherein each said chip is associated with a local event register, said local event register recording the occurrence of a hardware event associated with said chip.

Claims 20-21 (Cancelled).

22. (Currently amended) In an electronic device including at least one processor and a plurality of chips, each said chip associated with a local time counter of a plurality of local time counters, a medium ~~holding~~ comprising computer-executable instructions for a method comprising: ~~steps for a method, said method comprising the steps of~~:

detecting an event associated with one of said plurality of chips;

generating a timestamp with said local time counter at the time of the occurrence of said detected event, said timestamp being associated with said event; and

comparing said event and a normalized form of said timestamp with other events and associated normalized timestamps to determine an order of occurrence.

23. (Currently amended) The medium of claim 22 wherein said method further comprises ~~the further steps of~~:

providing a Time Base selected by said processor, said Time Base being a baseline time value; and

transmitting a reset instruction from said processor to said plurality of local time counters associated with said plurality of chips, said plurality of local time counters resetting to a designated time so as to be synchronized with respect to each other.

24. (Currently amended) The medium of claim 23 where said processor maintains a record of ~~the~~ an offset between the reset value of the local time counter and the Time Base.

25. (Original) The medium of claim 23 wherein said designated time is the Time Base and said plurality of local time counters are reset so as to indicate the same time as said Time Base.

26. (Original) The medium of claim 23 wherein the transmitting of said reset instruction is performed using a simultaneous multicast write operation performed by said processor.

27. (Currently amended) The medium of claim 23 wherein the transmitting of the reset instruction is staggered so as to ensure that said resetting occurs simultaneously, said transmitting taking into account ~~any~~ delays caused by network topology.

28. (Currently amended) The medium of claim 23, wherein said method further comprises ~~the further steps of~~:

resetting all of said plurality of chips and an additional chip~~-~~, said resetting being performed to add the ~~an~~ additional chip that is synchronized with said plurality of chips.

29. (Currently amended) The medium of claim 22, wherein said method further comprises ~~the further steps of~~:

providing a Time Base in a location accessible to said processor, said Time Base being a baseline time value;

determining an offset between the time indicated by said Time Base and the time indicated by each of said local time counters associated with said plurality of chips;

recording each offset associated with each said local time counter at a location accessible to said processor; and

normalizing the timestamps associated with said detected events using offsets associated with the local time counter generating the timestamps prior to determining said order of occurrence.

30. (Currently amended) The medium of claim 29, wherein said method further comprises ~~the further steps of~~:

determining an offset for an additional time counter associated with an additional chip in said electronic device following the initial determination and recording of said offsets for said plurality of local time counters associated with said plurality of chips; and

recording said offset at said location accessible to said processor.

31. (Currently amended) The medium of claim 22, wherein said method further comprises ~~the further steps of~~:

providing a Time Base selected by said processor, said Time Base being a baseline time value;

determining an offset between the time indicated by said Time Base and the time indicated by each of said local time counters associated with said plurality of chips;

transmitting each said offset for a local time counter to the chip with which the local time counter is associated;

recording each offset associated with each said local time counter at a location accessible to the chip associated with the local time counter; and

normalizing said timestamp using said offset associated with the local time counter prior to reporting said timestamp and said event to said processor.

32. (Original) The medium of claim 22 wherein a software timestamp received from the operating system is associated with said reported event and timestamp.

33. (Original) The medium of claim 32 wherein said software timestamp is used in determining said order of occurrence of events.

34. (Original) The medium of claim 22 wherein an indication of said detected event is stored in a local event register.

35. (Original) The medium of claim 22 wherein more than one of said plurality of chips is associated with the same local time counter.

36. (New) A method, comprising:

providing a baseline time value selected by a processor;

detecting an error on a first chip, wherein the first chip is controlled by the processor;

generating a first timestamp upon detecting the error on the first chip, wherein the first timestamp is generated by a first local time counter resident on the first chip;

forwarding the first timestamp to the processor;

normalizing the first timestamp with respect to the baseline time value;

detecting an error on a second chip, wherein the second chip is controlled by the processor;

generating a second timestamp upon detecting the error on the second chip, wherein the second timestamp is generated by a second local time counter resident on the second chip;

forwarding the second timestamp to the processor;

normalizing the second timestamp with respect to the baseline time value; and

comparing the normalized first timestamp with the normalized second timestamp to determine if the error on the first chip occurred before the error on the second chip.

37. (New) The method of claim 36, wherein the processor normalizes the first timestamp after the first timestamp is forwarded to the processor.